IC-EMC, a Demonstration Freeware for Predicting Electromagnetic Compatibility of Integrated Circuits

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***Abstract*— The freeware entitled IC-EMC is a windows-based software demonstrator which aims at simulating parasitic emission and susceptibility of integrated circuits. The following paper describes the main simulation features of this tool through several examples.**

I. INTRODUCTION

Simulation approaches for Electromagnetic Compatibility (EMC) evaluation have become critical to shorten design cycles of modern integrated circuits (IC). The knowledge in integrated circuit modelling has risen rapidly over the past ten years, mainly from the viewpoint of parasitic emission. Integrated Circuit manufacturers and customers have also started to use specific EMC prediction tools with reasonable success. However, the knowledge on EMC at component level is still a matter of a few experts. Real-case measurements and models are mostly confidential, which jeopardize the share of general knowledge on this topic. At the interface between IC designers and vendors, there is no tool available to exchange standard models or measurements in a convenient way. Also, trainings in university and industry are often conducted on a formal basis, using traditional EMC text books or very focused books on EMC of ICs [1].

In an attempt to break the ice and convince both IC designers and electronic designers to share EMC-related concerns and solutions, we developed a freeware platform called IC-EMC, a unique tool dedicated to the simulation of emission and susceptibility prediction at integrated circuit level [2]. The tool is also used for training in academic institutions, continuing education and engineer training in industry with outstanding impact. This paper aims at describing in more details the main features of this tool and highlighting the different innovative parts proposed on immunity, near field scan and chip-to-chip coupling simulation.

II. GETTING STARTED WITH IC-EMC

The tool IC-EMC [3] firstly aims at simulating parasitic emissions of integrated circuits. The tool uses the freeware WinSpice [4] derived from SPICE Berkeley for analog simulation. Several examples of comparison between measurements and simulations for various commercial and test ICs are proposed, within the range 1 MHz – 10 GHz. Innovative parts on immunity, near field scanning and chip-to-chip coupling simulation are also proposed. The main screen of the schematic editor is shown in Fig. 1. The editor contains a palette of symbols to build the schematic diagram of the circuit and the main processing tool icons.

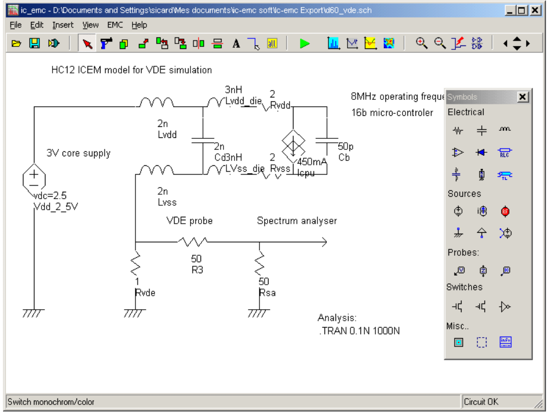

Fig. 1 The IC-EMC initial screen with a 32-bit micro-controller model

III. EMISSION PREDICTION

IC-EMC aims at simulating parasitic emission of an IC and comparing the results with conducted and radiated mode measurements according to international standard methods described in [5], more specifically 1/150 Ω and TEM/GTEM methods.

A. *Flow for emission prediction*

The global flow for emission prediction using IC-EMC and WinSpice is outlined in Fig. 2. An IBIS [6] model and an ICEM [7] model of the component under test are built. The IBIS file contains I/O and package information. Using WinSpice, the circuit is simulated in time-domain to get the on-chip and off-chip current/voltage variations. Then, different post-processing tool are applied, as Fast Fourier Transform (FFT) algorithm to obtain emission spectrum.

B. *Emission Simulation and comparison with Measurements*

The IC models proposed as examples follow the ICEM approach as described in IEC standard related to IC emission [5]. The schematic diagram is converted into a SPICE-compatible text file. The voltage waveform computed by the analog simulator WinSpice is translated into frequency domain by a FFT. The X axis covers the range 1 MHz - 10

GHz in logarithmic scale. The representation of the energy on the Y axis is given in dBµV. The spectrum appears as shown in the Fig. 3. Measurements are superimposed to the simulation for comparison purpose. The case-study proposed here concerns the conducted emission of a 32-bit micro-controller for automotive applications measured according to the standard IEC61967-4 (1/150 Ω) [8].

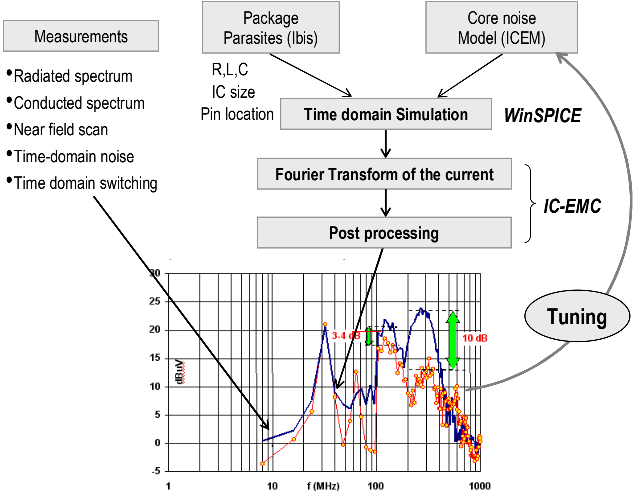

Fig. 2 Emission simulation flow using IC-EMC and Winspice

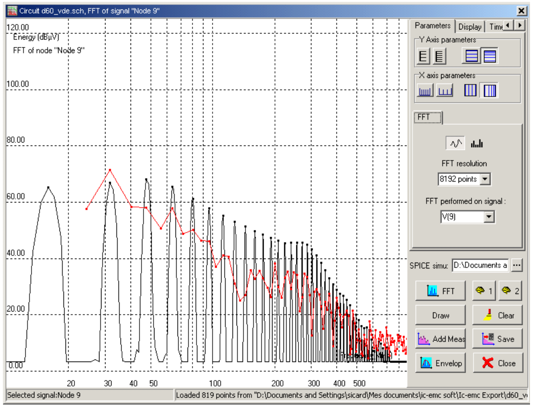

Fig. 3 Comparison between measured and conducted emission of a 32 bit micro-controller

IV. NEAR FIELD SCAN PREDICTION

The near-field scan method has been developed to perform near-field electromagnetic emission map. It allows identifying and localizing radiating sources at the surface of a PCB or an IC [9] [10].

A. *Key role of IBIS file for package modeling*

The key assumption made for the near-field prediction is that leads and bonding of package are considered as the main radiated elements at IC level. Therefore a model of IC package is required to predict IC near-field radiated emission. Geometrical elementary information added in IBIS file enable package model construction. IBIS has been chosen since it is a common and standard format used to exchange information about I/Os and package electrical parasitics. The 3D package viewer gives a three-dimensional interactive view of the package from its IBIS description based on a reduced set of package geometrical parameters. An example of 3D view of a BGA package is given in figure 4.

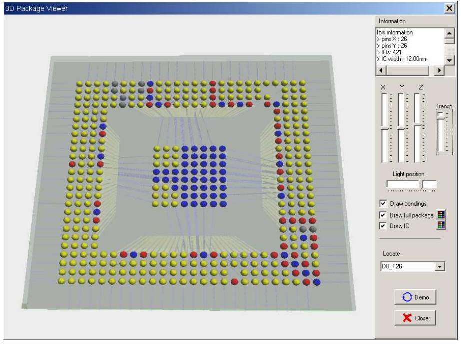

Fig. 4 3D-package viewer based on IBIS

B. *Flow for near field scan prediction*

Figure 5 describes the general flow for radiated near-field scan emission. The IBIS file is loaded, from which pin list, package dimension and type are extracted in order to build a geometrical model of the package. Then each package lead is associated to a position in space. Leads appear like inductance on the electrical schematic of the circuit. Each inductance associated to a package lead is assigned to the corresponding space coordinates in order to link the electrical schematic and the geometrical model of the package. Currents flowing in each declared package inductances are computed by WinSPICE. Then magnitudes of these currents are extracted for any scan frequency by IC-EMC FFT algorithm. Finally quasistatic approximation formulations are used to compute the sum of magnetic field contributions at any location of space. A post-processing displays the resulting magnetic field at the user-defined distance above the ground plane.

C. *Near field scan simulation and comparison with measurements*

Figure 6 presents a comparison between a measured and a simulated H_y component of magnetic field scan measured 200 µm above the surface of a 16 bit microcontroller at the harmonic frequency of its core activity [11]. Radiating areas are located along ground pins of the package. Peak values of magnetic field have been superimposed on scan results.

V. IMMUNITY PREDICTION

IC-EMC also performs susceptibility simulations of an IC to external radiofrequency interference (RFI) and compares the results with conducted and radiated mode measurements according to international standard methods described in [12], more specifically DPI, BCI and TEM/GTEM methods.

A. *Flow for immunity prediction*

The general flow used to achieve a comparison between susceptibility measurement and simulation is described in figure 7. On one side, the immunity measurement is performed using the standardized test bench [12]. The result is given in terms of power in dB-milliwatt (dBm) versus frequency. To build the model of the DUT aggression, we rely on package information given by IBIS, core model given by ICEM, and the injection path model including the RFI generator, the cable, the coupler the coupling capacitance and all the tracks on the PCB on which the tested component is mounted. The disturbance level is increased linearly for a given frequency during all the simulation duration thanks to a sinusoidal programmable source. At the end of the simulation, values of forward and reflected powers are extracted when the defined susceptibility criterion is reached. The predicted susceptibility threshold is then built by iterating this process for several frequencies.

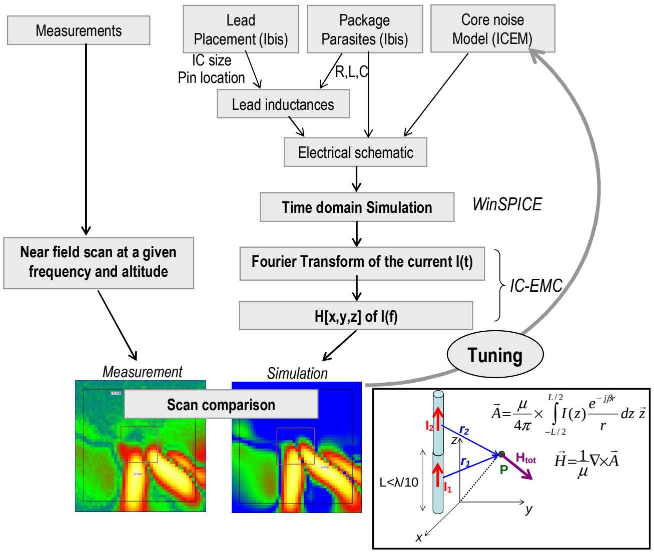

Fig. 5 Near-field scan simulation flow using IC-EMC and Winspice

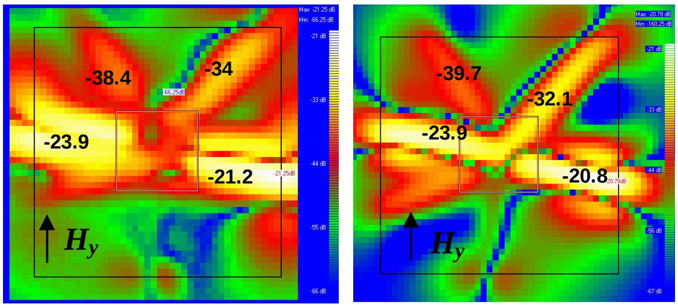

Fig. 6 Comparison between measurement (on the left) and simulation (on the right) of radiated H_y magnetic field above the surface of a 16 bit microcontroller (dark color = low amplitude, light color = high amplitude)

B. Example of immunity prediction

Several parts are essential for the accurate modeling of the IO susceptibility. The RF disturbance flows from the RF source to the amplifier, through the coupler, the DPI capacitor, the printed-circuit-board tracks, the package lead, bonding and eventually to the buffer. Figure 8 presents an example of model of susceptibility prediction for an I/O port of a 16-bit microcontroller to a conducted disturbance. Figure 9 presents the measurement results in terms of forward power versus frequency [13]. The maximum injected power is around 25 dBm. The simulation is also shown and exhibits very similar values to the measurements. The on-chip buffer is connected to its own supply network which propagates the injected noise within all the circuit.

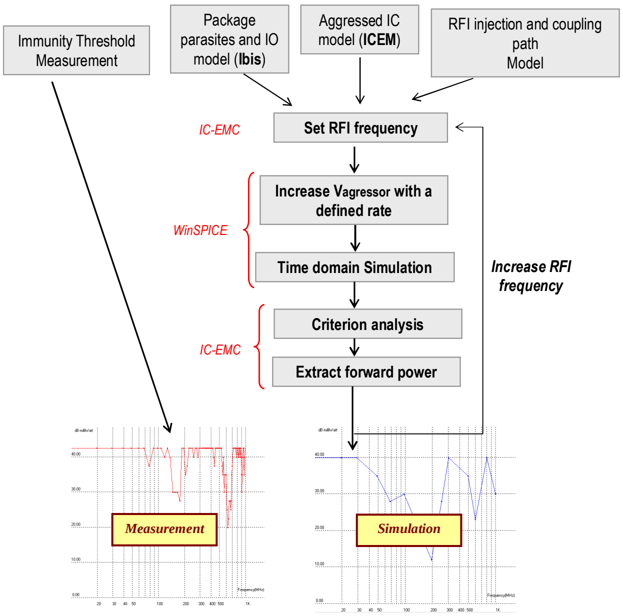

Fig. 7 Immunity simulation flow using IC-EMC and Winspice

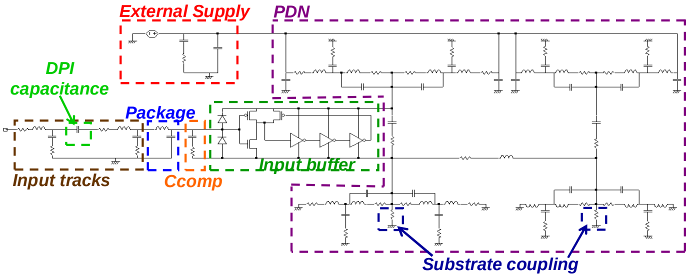

Fig. 8 DPI susceptibility model of on an input buffer of a 16-bit microcontroller

VI. CHIP-TO-CHIP COUPLING

In some applications as smart power device or front end radio frequency (RF) emitter, sensitive analog or digital ICs are placed close to “noisy” blocks like power amplifier or DC-DC converter. Disturbances due to mutual electromagnetic interferences (EMI) tend to increase with progresses in package and silicon integration [14]. A new feature recently added to the IC-EMC platform to enable the prediction of chip-to-chip coupling due to radiated mutual coupling. The proposed approach consists in extracting the electromagnetic coupling between ICs mounted in two different packages and evaluating disturbance risks due to mutual interferences.

A. General simulation flow

The general flow for chip-to-chip failure analysis is described in figure 10. Two ICs are considered: the first one is the source of disturbance, the other is the victim. Their respective IBIS files are loaded to build geometrical models for their packages. Then a 3D interface allows configuring their placement and pin assignation for coupling evaluation. A

Partial Element Equivalent Circuit (PEEC) method is used to extract coupling between package leads and bondings in term of partial inductance and capacitance matrix. Aggressor and victim models as well as extracted coupling values are mixed together to produce a complete electrical schematic diagram used to predict appearance of failure of the victim IC due to the proximity of the aggressor IC.

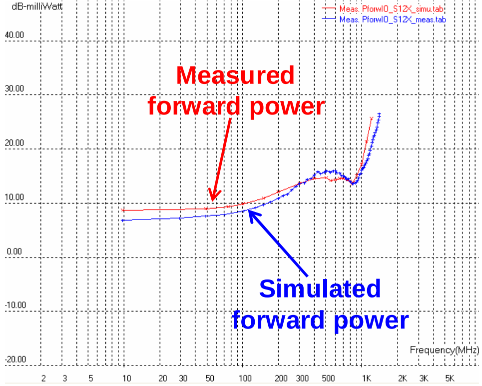

Fig. 9 Immunity results obtained on an input buffer of a 16-bit microcontroller

B. *Example of chip-to-chip coupling simulation results*

Figure 11 compares measurement results and simulation of failure levels induced on a analog-to-digital converter disturbed by a nearby power MOSFET switch. The X axis corresponds to the separation in millimetres between packages of both components, Y axis is the failure level of the victim ICs expressed in term of conversion error. The simulation curve obtained with IC-EMC correlates to the measured one.

VII. CONCLUSIONS

IC-EMC is a software dedicated to integrated circuit electromagnetic compatibility prediction. In this paper the main simulation features have been described, which concern conducted and radiated emission as well as susceptibility prediction. Moreover, some innovations have been proposed like the near-field scan simulation and the evaluation of failures induced by chip-to-chip EMC evaluation in the case of very complex stacked ICs. Further developments will concern chip-to-chip coupling and extend emission and susceptibility case study library. A training book around IC-EMC is also under consideration.

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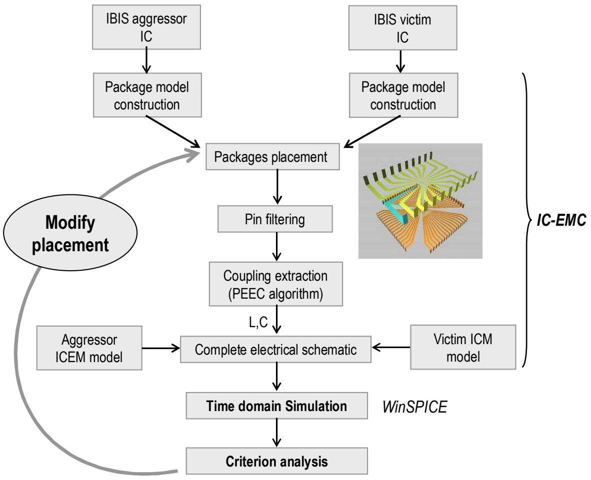

Fig. 10 Simulation of failure risks due to mutual interference in a chip-to-chip coupling using IC-EMC and Winspice

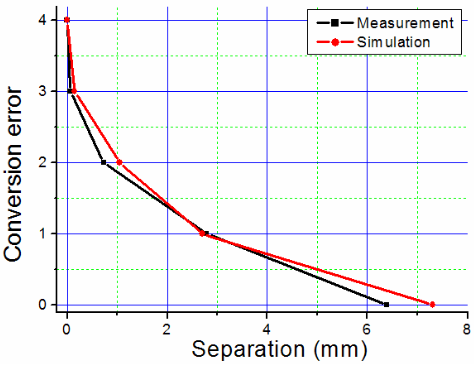

Fig. 11 Comparison between measured and simulated failure level for a analog-to-digital converter disturbed by a nearby power switch [15]