

# A Novel Software Environment for Predicting the Parasitic Emission of Integrated Circuits

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**Abstract:** This paper presents the tool IC-EMC, a Windows-based environment for the simulation of parasitic emission of integrated circuits. The tool consists of a dedicated schematic editor, a core activity evaluator, an IBIS translator and a dedicated post-processor. The core activity evaluator translates the integrated circuit specification into a noise source and a decoupling network. The IBIS translator gives information about the input/output characteristics and the package and supply model. A post processing features an immediate comparison of predicted and measured spectrum. IC-EMC handles a set of standards for integrated circuit modeling, emission modeling and test setups. The tool has been successfully used to modelize the parasitic emission of 16-bit, 32-bit microcontrollers, ASICs and programmable devices, within the range 1MHz-2GHz.

## 1 INTRODUCTION

Parasitic emission caused by the switching activity of integrated circuits has increased in importance with the tremendous progress in fabrication and packaging technology. According to the International Technology Roadmap for Semiconductors [1], the 45nm CMOS process will be made available for production in 2007, featuring a standard operating frequency near 10GHz for processing units, and the capability to integrate nearly one billion transistors. At each active clock edge, thousands of elementary current pluses are generated at gate level and provoke very important current flows within the chip. A comparison between 16-bit and 32-bit micro-controller current waveforms is given in figure 1. The peaks may be as high as 10 to 100A in the latest generation of high performance microprocessors.

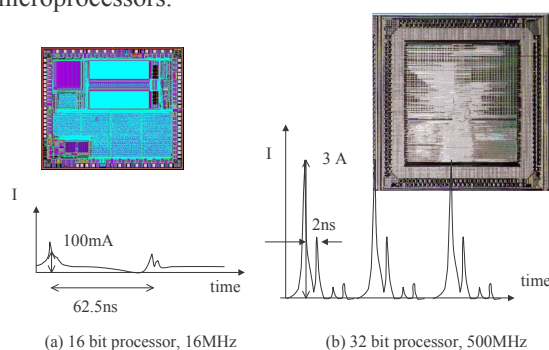


Figure 1. Internal current peaks of 32-bit micro-controllers may reach several Ampere

Due to these transient currents, the ICs may propagate important switching noise and radiated high levels of parasitic emission. In contrast, there is a growing

demand for low emission integrated circuits, especially in the automotive, mobile communications and aerospace markets. Several noise reduction techniques have already been proposed in technical papers and implemented successfully in industrial micro-controllers. Applying low emission design rules prior to integrated circuit fabrication requires accurate noise models, adequate simulation tools and a reliable emission prediction methodology.

This paper described a novel tool that aims at providing a simple, efficient and user-friendly environment to forecast conducted and radiated emission of integrated circuits. The tool is based on non-confidential standards such as IBIS [2] for I/O description and ICEM [3] for core description. Section 2 describes the general flow and section 3 details the ICEM model generator. Experimental case studies are described in part 4, and concern conducted and radiated emission. Details about near-field scan are reported in part 5, followed by a conclusion.

## 2 BASIC FLOW

The general flow for constructing an emission model and achieving a comparison between prediction and measurement is illustrated in figure 2. The package, I/O and supply structures of the circuit under test are described in IBIS format. In parallel, the electrical model of the core and supply decoupling networks are given in an ICEM format. The analog simulation is performed in time domain by a SPICE simulator such as WinSpice [4].

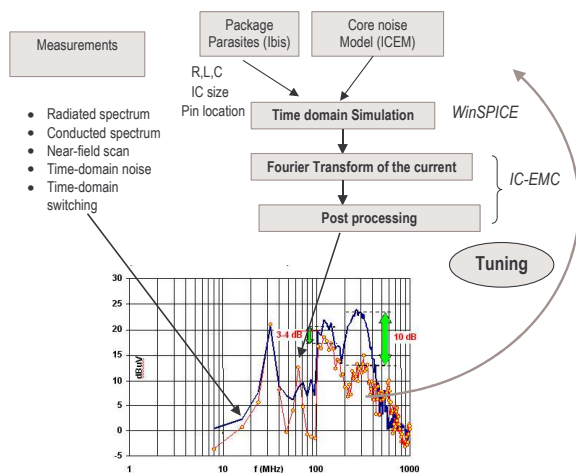


Figure 2. Methodology implemented in IC-EMC to compare measured and simulated emission

The Fourier Transform and EMC post-processing are embedded in IC-EMC. The main commands of tool are shown in figure 3. From left to right, the Spice Simulation icon translates the schematic diagram into a SPICE compatible text file, the other icons give access to the emission spectrum window, the impedance vs. frequency, the immunity simulation screen, and the near-field simulation screen.

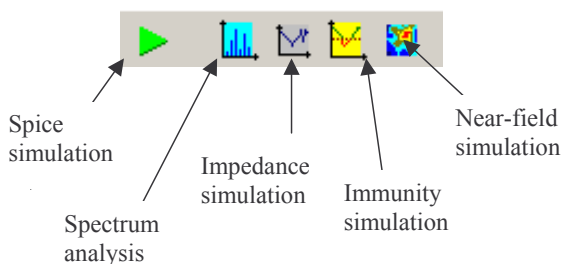


Figure 3. The main tools provided in IC-EMC

### 3 CORE NOISE MODEL GENERATION

This section describes the principles for generating generic ICEM models from high-level specifications of the integrated circuit technology, topology and gate complexity.

#### 3.1 EMC EXPERT

The ICEM model expert interface is reported in figure 4. On the left upper corner of the window the default technological parameters are listed, namely the typical switching current per gate (0.3mA in this technology), the typical duration of the gate switching (100 ps), and the default parasitic capacitance between VDD and VSS for each gate (7fF).

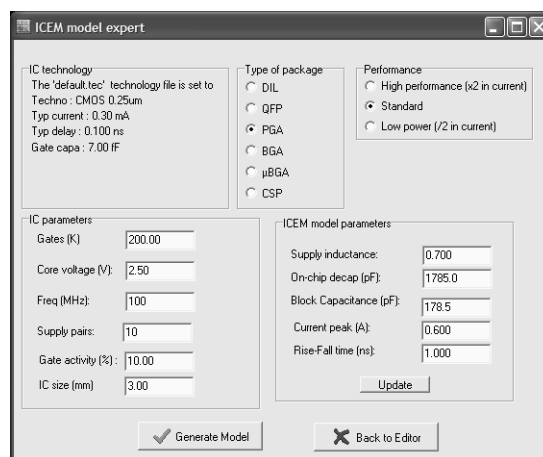


Figure 4. The ICEM model generator and its user's interface

The menu “Type of package” lists some packaging technologies. The “performance” menu tunes the switching current peak according to the technological option : 50% increase in “high speed” mode as compared to standard mode, 50% decrease in “low power” mode. In the lower left corner, important parameters that have a direct impact on the ICEM model are given:

- The number of gates (200K gates in the example)
- The operating frequency (100MHz)
- The supply pairs, i.e the number of VDD/VSS pins (10)
- The % of switching activity in each active edge of the clock (10%)
- The IC size in mm (3x3mm)

A result example corresponding to the default expert system parameters is given in figure 5. The current generator  $I_b$  is situated on the right side, with its local block capacitance. The serial access resistance  $rdie\_vdd$  and inductance  $ldie\_vdd$  link the noise source to the decoupling capacitance  $Cdec$ , which is connected to the supply inductance  $lpack\_vdd$ .

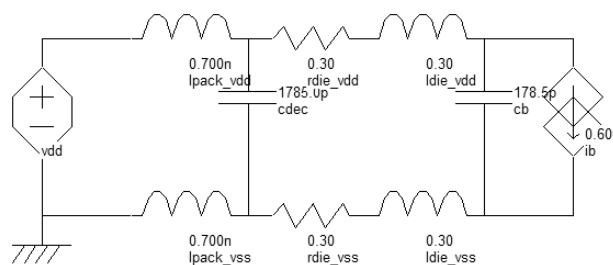


Figure 5. An example of ICEM model generated by IC-EMC from technological specifications

TABLE I. ANALYTICAL FORMULATIONS USED TO GENERATE THE ICEM MODEL PARAMETERS

$L_{die\_vdd}$ $ic\_Size*inductanceFactor$ ; $R_{die\_vdd}$ $ic\_Size*resistanceFactor$ ;	=	The serial inductance and resistance are proportional to the size of the die. The factors are around 0.1, if the ic size in in mm.
$imax=icPerfo*Gates*typ\_current*$ $Gate\_Activity/spreadFactor$ ;	=	The peak current of the source $I_b$ is compute using several parameters: the spread factor is around 10; $icPerfo$ is equal to 2 for high performance, 1 for standard and 0.5 for low power option.
$tr := typ\_Delay*SpreadFactor$ ;	=	The rise and fall time of the current source is multiplied by the spread factor.
$L_{pack\_vdd}$ $:=L\_package/SupplyPairs$ ;	=	The serial inductance is divided by the number of pairs. The inductance per pin depends on the package technology (15nH for DIL down to 1nH for CSP).
$C_d := Gate\_Capa*Gates+$ $icSupplyPairs*ioCapa+$ $icSize*icSize*SurfaceCapa$ ;	=	The decoupling capacitance is the sum of the gate capa, the lo capa and the die surface capacitance.
$C_b := Cd/10$	=	The local block capacitance $C_b$ is 10 times lower than the total capacitance

The computation of the ICEM elements is performed using the assumptions listed in table 1. The package and die size information have a direct impact on the amount of on-chip parasitic capacitance, on-chip and off-chip supply inductances. The current source is assigned a time-dependent value for transient analysis. The main noise source  $I_b$  is evaluated from the peak current formulation which combines the typical current, the number of gates, a factor depending of the technology performance, and a spreading factor that accounts from the non-synchronous behavior of the switching.

### 3.2 SIMULATION

The simulation is performed in time domain (.TRAN analysis), with duration around 1000NS and a resolution of 0.1NS, that enables to compute its spectrum from 1MHz to 5GHz. A typical plot of the transient simulation is reported in figure 6, corresponding to the conducted emission of a 32-bit processor TriCore.

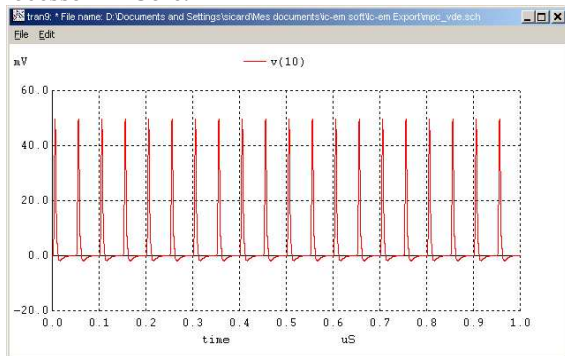


Figure 6. The transient simulation performed by WinSpice

### 3.3 POST-PROCESSING

A Fast Fourier Transform (FFT) converts the voltage waveform computed by the analog simulator into frequency domain energy. The representation of the energy in Y axis is proposed in  $\text{dB}\mu\text{V}$ , equal to  $20*\log(V*1^6)$ , as shown in figure 7. Simulated (black) and measured (envelop) conducted emission shown in the figure concern a 32-bit micro-controller for automotive applications.

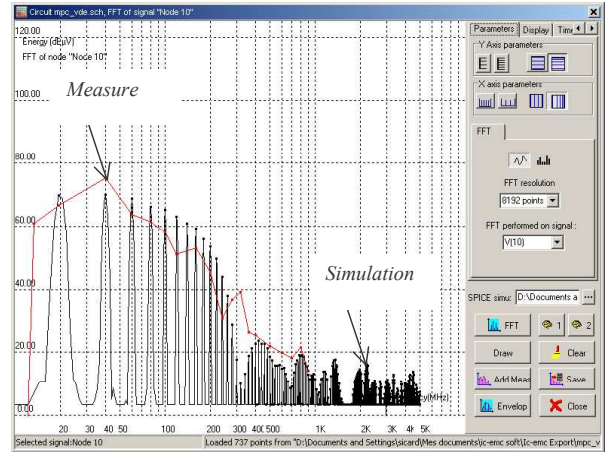


Figure 7. Comparison between measured and conducted emission of a 32-Bit processor

### 3.4 RADIATED MODE

In radiated mode, two main coupling phenomena have been identified: the capacitance coupling between the die and the inner metal plate of the TEM or GTEM (Called septum), and the inductance coupling between the package and the septum. The capacitance coupling between the IC and the septum is represented by  $C_x$ , with a value of 30fF (Figure 8). The inductance coupling between the VDD supply inductance  $L_{vdd}$  and the septum inductance  $L_{tem1}$ ,  $L_{tem2}$  is represented by a coupling factor K. The coupling value is usually the order of 0.1 to 1%.

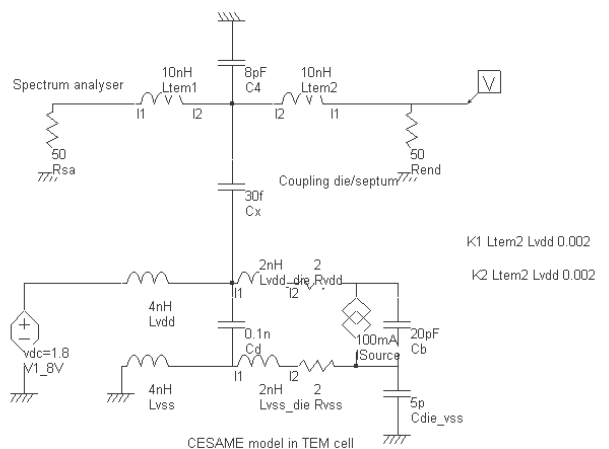


Figure 8. A coupling model between an integrated circuit and the septum of the TEM cell

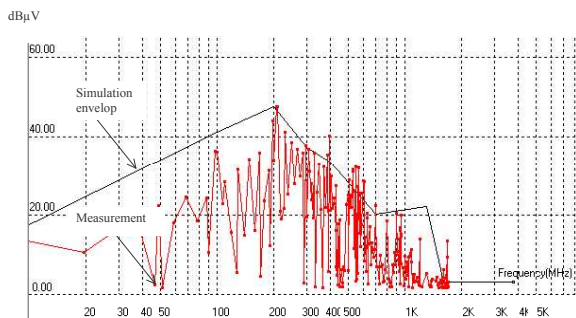


Figure 9. Comparing simulation and measurements of the CESAME test chip [5] in the TEM cell.

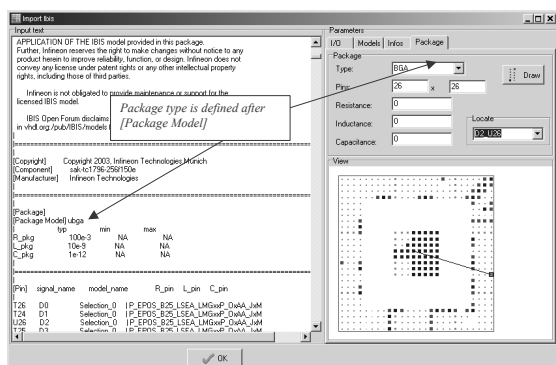


Figure 10. Package viewer based on IBIS

A comparison between measurements (spectrum in red) and simulation (Envelope in black) is proposed in figure 9. It can be seen that a reasonable agreement is found up to 1GHz for this test chip [5]. The simulation is significantly higher than measurements above 700MHz. Notice that the I/O switching that occurs in real-case measurements at a rate of 10MHz provokes a series of harmonics.

The tool may also be used for mixed signal circuits or multiple-supply ICs. In [9], IC-EMC was successfully used to modelize multiple supply networks with separated I/O and core decoupling.

#### 4 THE ROLE OF IBIS

The IBIS information is of crucial importance to accurately describe the emission model parameters of the integrated circuits. The added value of IBIS information is its ability to simulate the transient switching of the input/output signals. Furthermore, the list of pins is also described in IBIS, which enables IC-EMC to reconstruct the package pin assignment and consequently evaluate with a reasonable accuracy the parasitic electrical parameters of the package leads. The example shown in figure 10 concerns a TriCore micro-controller mounted on a BGA from Infineon (TC1796 AUDO [6]).

#### 5 NEAR-FIELD SCAN PREDICTIONS

The near-field scanning prediction is based on elementary current dipole formulations associated to each supply package inductance of the integrated circuit [7].

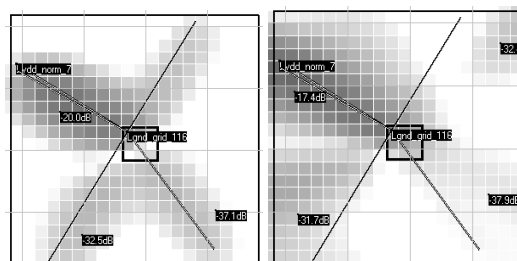


Figure 11. The simulated (left) and measured (right) magnetic emission of the CESAME test chip

The tool IC-EMC includes the analytical formulations to reconstruct the near field ( $H_x$ ,  $H_y$ ,  $H_z$ ,  $H_{total}$ ) at a given altitude, and provides the user with an interface to ease the comparison with measurements. Good correlations between measurements and simulation have again been obtained for several test-chips (Such as CESAME in figure 11) and industrial micro-controllers such as C51, HC12 and S12X. However, all these devices used conventional QFP packaging. The adequacy of this approach for BGA and CSP packaging remains unknown.

#### 6 CONCLUSION

This paper has described a software that aims at regrouping in a single environment specific tools for modeling and predicting the parasitic emission of integrated circuits. The software has proven very efficient at creating IC models for micro-controllers and ASIC circuits, applicable for both conducted and radiated emission. Future developments will concern immunity and systems-in-package EMC.

The tool has been developed within the frame of the European project MEDEA+ "Mesdie" A-509. The full package, a 100 pages documentation and several test case examples are freely available at the web address [8].

#### REFERENCES

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